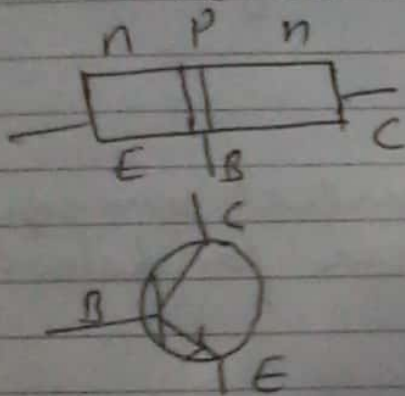
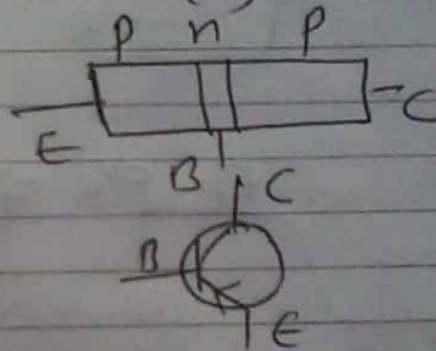


Bipolar Junction Transistor.

When a layer of n-type Si is sandwiched between two layers of p-type Si, a Pnp transistor is formed. If p-type Si is sandwiched between two n-type Si, an npn transistor is obtained. The middle of the sandwich is called the base (B) and the two ends are called emitter (E) and the collector (C).



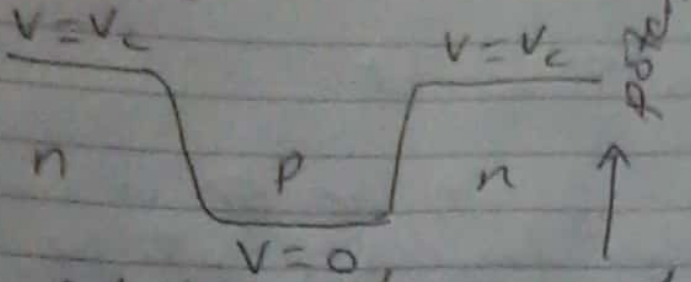
Symbol of npn



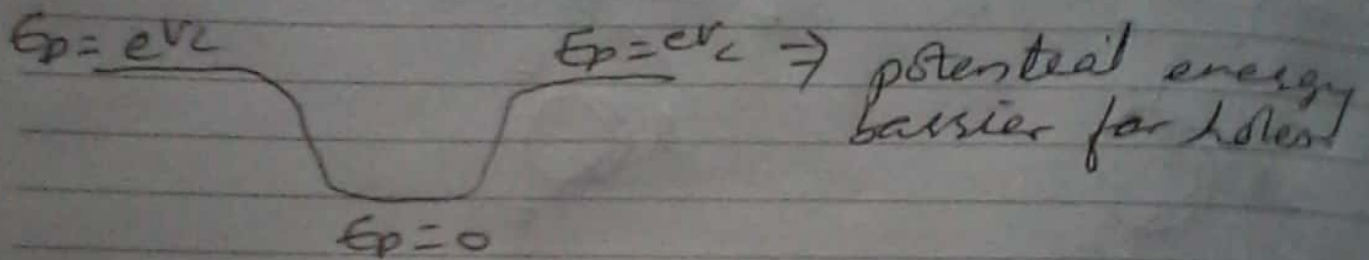
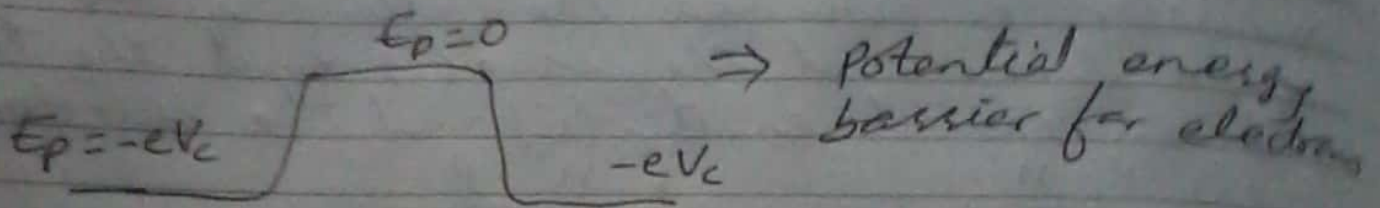
symbol of pnp.

The base of transistor is very thin and very lightly doped. The emitter is heavily doped and thickness is moderate. It's function is to emit majority charge carriers. The collector is moderately doped and thickest layer. It's function is to collect majority charge carriers emitted by emitter.

When the three semiconductor layers are put together, majority carriers will flow across the two junctions, creating contact P.D. between the emitter and base and between the collector and the base.



p.d betⁿ three parts of transistor.



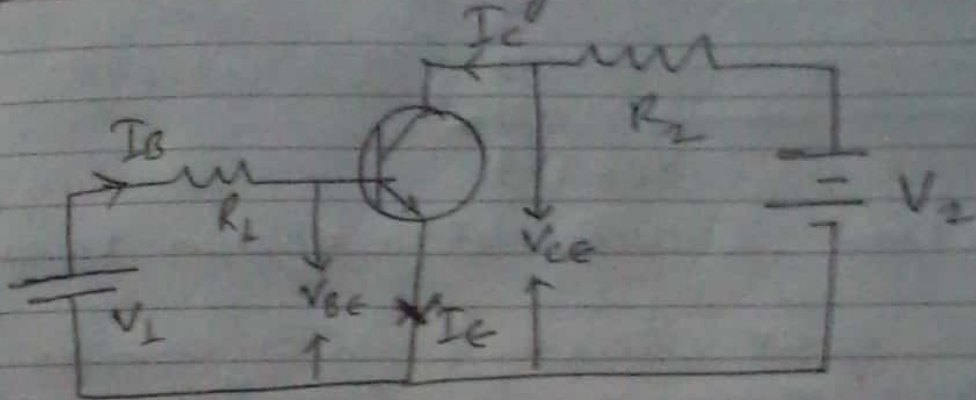
Modes of configuration

There are different modes of configuration of transistors. They are
 ① CE mode ② CC mode ③ CB mode

For proper functioning of transistor the base-emitter junction should be forward biased and the base-collector junction should be reverse biased.

Common ~~base~~ emitter configuration

It is the most common configuration in which emitter is common to both the input and the output circuit.

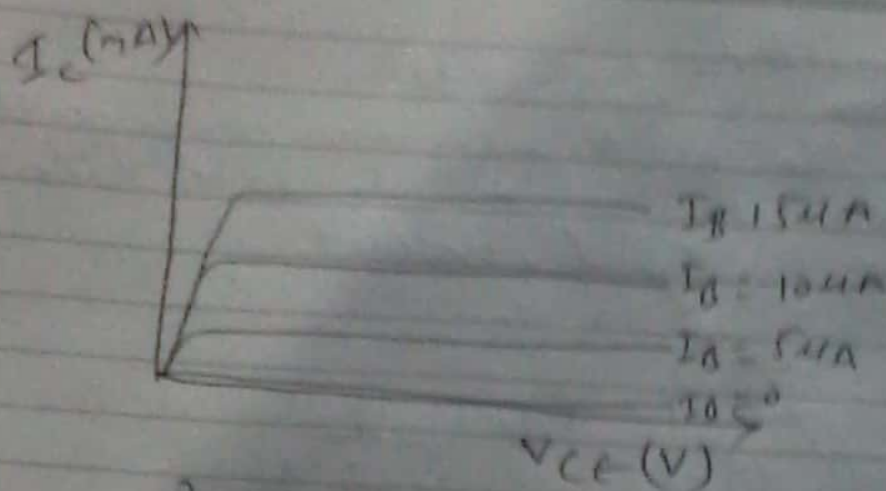


CE mode of npn transistor

Here the base-emitter junction is forward biased. In output branch battery V_2 and the load resistance R_2 are connected along with the collector-base junction and emitter-base junction. The potential of collector is higher than that of the emitter by an amount $V_{CE} = V_2 - I_C R_2$. The nature of the bias at the collector-base junction will depend on the relative values of the V_{CE} & V_{BE} .

In CE mode, the input current I_B and the output current I_C are independent and dependent variables respectively.

The output characteristics of npn transistor in CE mode is shown in fig below.



Output characteristics of npn transistor

The output characteristics can be divided into active region and saturation region. The active region is to the right of the knee of the curve. In this region I_C is very sensitive to I_B but almost independent of V_{CE} . The saturation region is the left of the knee. In this region I_C increases sharply with V_{CE} .

From circuit diagram we have

$$I_E = I_B + I_C$$

$$\text{or } I_E \approx I_C \text{ as } I_B \text{ is negligible.}$$

Using $\alpha = \frac{I_C}{I_E}$

$$\alpha = \frac{I_C}{I_C + I_B}$$

$$\alpha = I_C \left(\frac{1}{I_C + I_B} \right) = I_B$$

$$\alpha = I_C = \beta I_B \text{ where } \beta = \frac{\alpha}{1-\alpha}$$

is called current gain parameter

The value of α is very less than the value of β is very high. Thus the common emitter circuit is used in the active region, it acts as a current amplifier.

Amplification using bipolar transistor

In the circuit diagram of CE mode we have from Kirchhoff's laws.

$$V_{in} = V_1 = R_1 I_B + V_{BE} \quad \&$$

$$V_{CC} = V_2 = R_2 I_C + V_{CE}$$

Since transistor operates in the forward active mode we have $V_{BE} = 0.7V \quad \&$

$$I_C = \beta I_B$$

Combining these relations we get

$$V_{out} = V_{CE} = V_{CC} - \beta \frac{R_2}{R_1} (V_{in} - 0.7V)$$

Thus any variation of the input voltage ΔV_{in} corresponds to the variation of the output voltage. The variation is proportional to ΔV_{out} . Since

$$\Delta V_{out} = - \beta \frac{R_2}{R_1} \Delta V_{in}$$

$\therefore$ The output signal is equal to the input signal multiplied by a voltage amplifier's factor $\beta \frac{R_2}{R_1}$. -ve sign

indicates a 180° phase

If $V_{CE} = R_L I_C = +V_{CE}$ is multiplied by I_C
we get $I_C V_{CE} = R_L I_C^2 + I_C V_{CE}$.

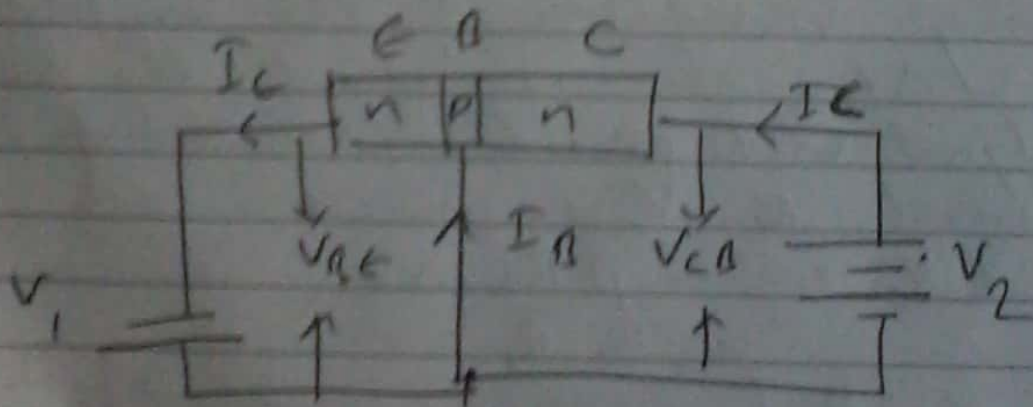
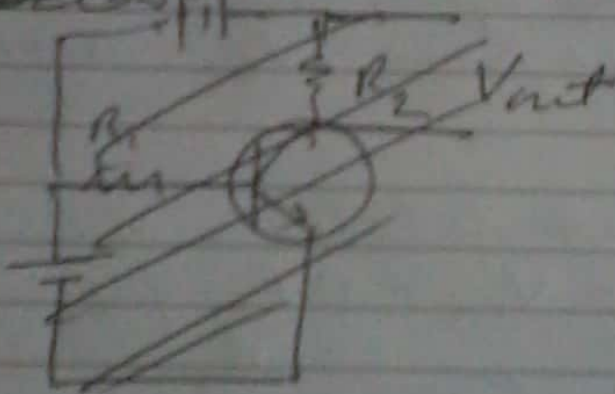
Here $I_C V_{CE}$ = power supplied by the source

$R_L I_C^2$ = power dissipated in the load resistor

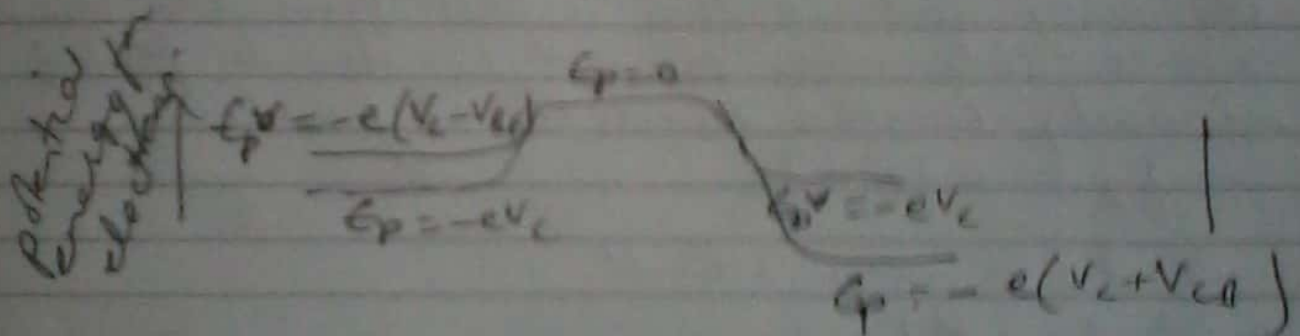
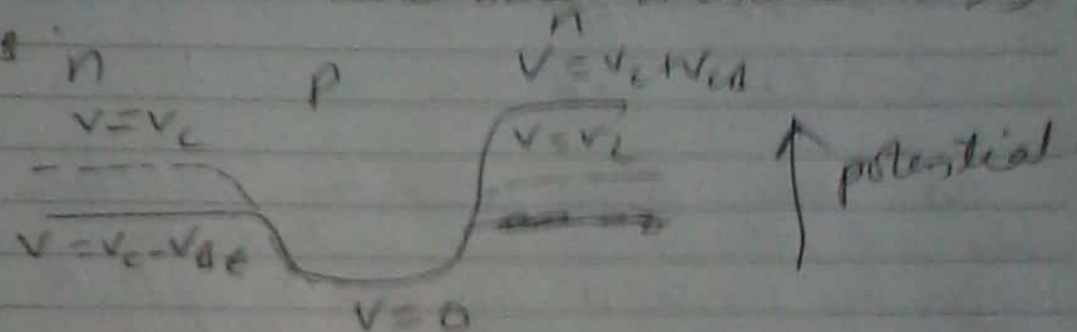
$I_C V_{CE}$ = power dissipated in the transistor.

Common base configuration.

The circuit diagram for CB mode as shown below:

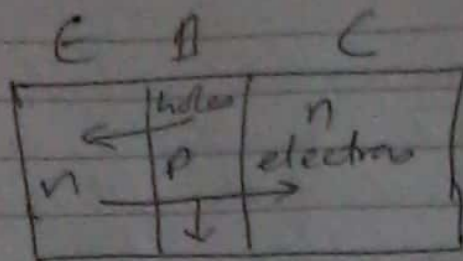


Since base is common to input and output it is called CB mode. In the circuit V_i will raise the potential of the p-type base relative to n-type emitter. Thus pd betⁿ the emitter and base is reduced to $V_c - V_{be}$. On the other hand V_i lowers the potential of the base relative to the collector by V_{be} & pd betⁿ collector and base is increased by $V_c + V_{be}$.



Due to forward biasing at emitter-base junction, electrons move from emitter to base and the holes move from base to emitter.

The electrons that reach at base neither recombine with holes in base nor flow through the lead of base but they reach to collector junction and due to $V_c + V_{be}$ potential they accelerate across the gap collector.



Here I_E = emitter current

I_C = collector current

I_B = base current.

$I_E = I_{EE} + I_{BE}$ but $I_{BE} \ll I_{EE}$

$\therefore I_E \approx I_{EE}$

As the base collector junction is reverse biased, there is no contribution from the majority carriers in base & collector to I_C .

The only contribution is that from the small reverse saturation current I_0 due to flow of minority carriers across the CB junction.

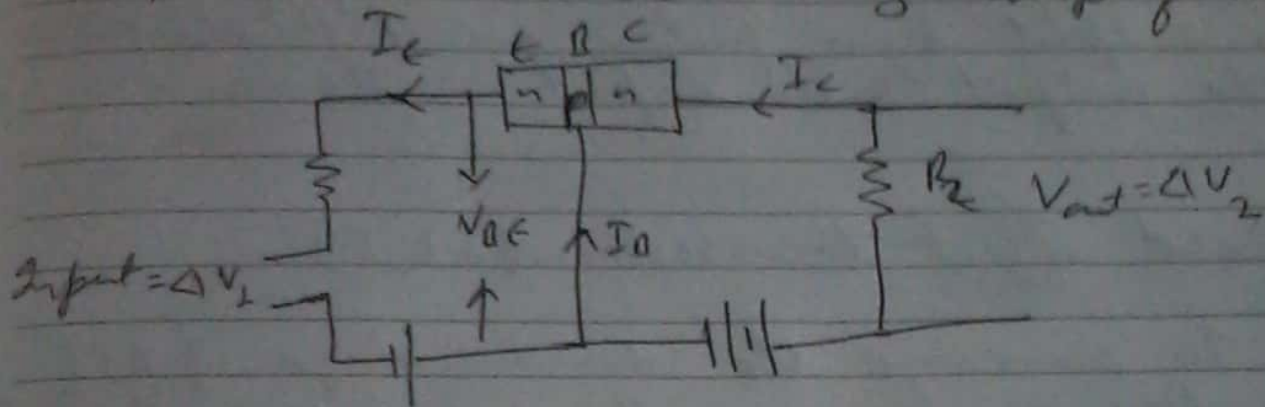
$I_C = \alpha I_E + I_0$

I_0 is very small

$\therefore I_C = \alpha I_E$

The collector current is essentially determined by the emitter current, which is determined by P.d across B & E i.e. V_{BE} . I_C is almost independent of V_{CE} .

The transistor as a voltage amplifier



Here R_1 is small resistance introduced in emitter base circuit and R_2 is large resistor. The emitter base junction is forward biased and collector base junction is reverse biased.

The input is given in EB junction by applying a voltage ΔV_1 & output voltage is taken across the resistor R_2 .

From circuit:

$$\Delta V_1 = \Delta I_E (R_1 + R_e) \quad \Rightarrow \quad \Delta I_E = \frac{\Delta V_1}{R_1 + R_e}$$

where R_e = effective resistance of EB junction

$$\therefore \Delta I_C = \alpha \frac{\Delta V_1}{R_1 + R_e}$$

The output voltage across R_2 is

$$\Delta V_2 = R_2 \Delta I_C = \alpha \frac{R_2}{R_1 + R_e} \Delta V_1$$

If $\alpha = 1$ we get

$$\Delta V_2 = \frac{R_2}{R_1 + R_e} \Delta V_1$$

Daily Notes

The ~~output~~ ^{input} voltage will be amplified at the output by a factor equal to the ratio of the output to the input resistances.

Field effect transistors (FET)

To overcome the disadvantage of BJT i.e. low resistance in the input circuit FET is introduced. There are two types of FET

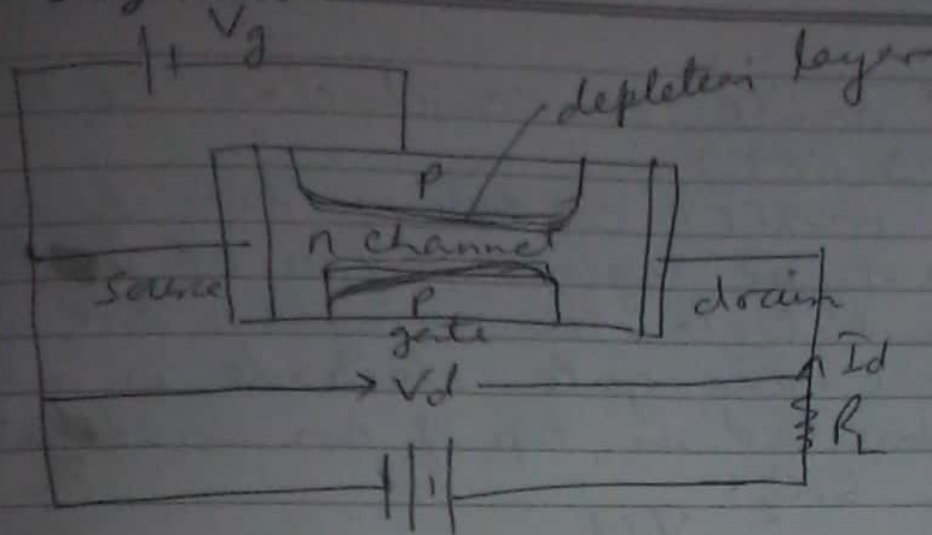
- ① Junction field effect Transistor
- ② Metal oxide semiconductor FET.

FET's have two salient features

- ① They are voltage controlled devices. The current through the device is controlled by the electric field associated with a voltage placed at an electrode called the gate.
- ② The current is transported by carriers of one polarity only (majority carriers), so called unipolar transistor.

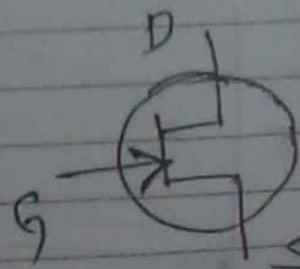
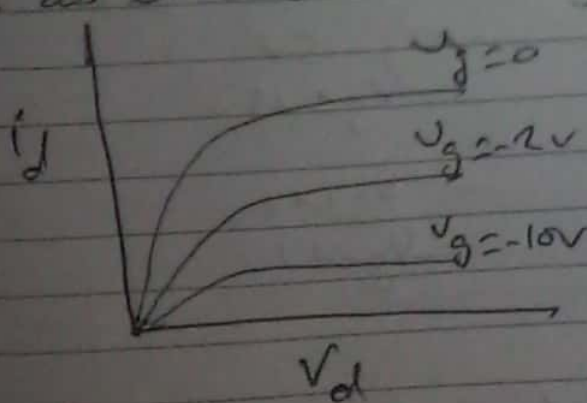
① JFET

It consists of a channel of a semiconductor to which two metallic ohmic contacts called source and drain are made. In N-channel JFET a heavily doped P-type semiconductor region called the gate surrounds the n-type channel.



In normal mode operation, the gate source is always reverse biased and source and drain are interchangeable. Source is connected in such a way that it emits majority charge carriers of channel.

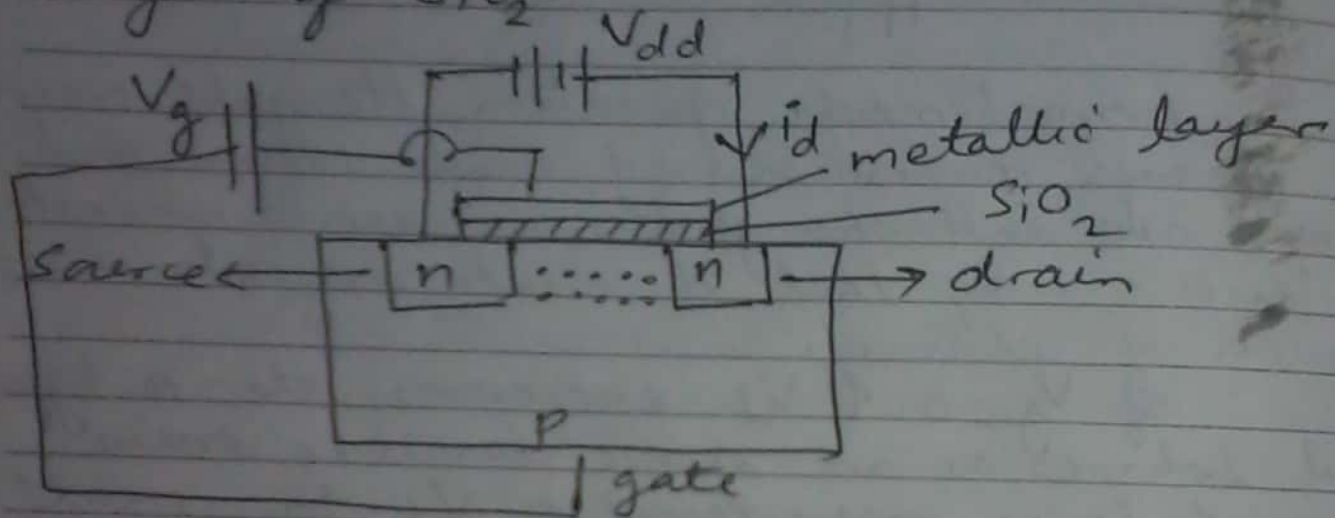
If $V_g = 0$ & V_d increases, the n-type rod behaves as an ohmic device i.e. drain current I_d is proportional to V_d . For small V_d depletion layer is formed and if V_d is increased, the p-n junction at the gate becomes more and more reverse biased. This has effect of increasing the resistance of the rod. Thus I_d does not increase so fast as it did initially, when V_d is small.



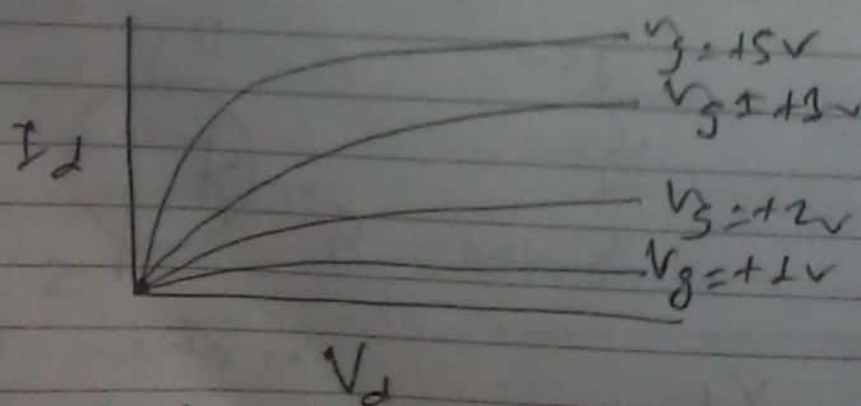
n channel FET.

Metal oxide semiconductor. FET (MOSFET)

→ The MOSFET consists of two heavily doped n-type regions diffused into a p-type substrate. Two n-regions are drain and source. The gate electrode is metallic layer deposited on top of an insulating layer of SiO_2 .



When $V_g = 0$, I_d will be zero. If V_g is increased, electrons from p-substrate are attracted toward SiO_2 interface. This provides a channel for the current I_d to flow from drain to source when V_d is applied. I_d increases with V_d .



Output characteristics of MOSFET